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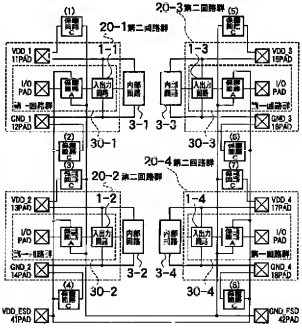
(54)【発明の名称】　静電破壊保護回路

(57)【要約】
【課題】　異種電源間の静電破壊保護用の保護回路の数を異種電源の数が増えても抑えること。
【解決手段】　入出力回路と信号入出力端子との間に挿入されて前記信号入出力端子から侵入する静電電圧より前記入出力回路を保護する第１の保護回路を複数の内部回路対応で設け、前記複数の第１の保護回路全てに対して独立した共通対電源端子から電源を供給するようにし、前記複数の内部回路にそれぞれ電源を供給する複数の対電源の各ＶＤＤ側端子に一方の電源端子を接続し、他方の電源端子を前記共通対電源端子のＧＮＤ側端子に接続するか、又は前記複数の対電源の各ＧＮＤ側端子に一方の電源端子を接続し、他方の電源端子を前記共通対電源端子のＶＤＤ側端子に接続して前記内部回路を静電電圧より保護する第２の保護回路を前記複数の対電源対応で設けることにより前記第２の保護回路の数を異種電位電源の数が増えても増加しないようにする。



【特許請求の範囲】

【請求項１】　対電源端子から電源が供給され、且つ外部の信号入出力端子に対し信号を入出力回路を介して入出力する内部回路を複数個有する回路にあって、前記入出力回路及び前記内部回路を外部から侵入する静電電圧による破壊から保護する静電破壊保護回路において、

前記入出力回路と前記信号入出力端子との間に挿入されて前記信号入出力端子から侵入する静電電圧より前記入出力回路を保護する回路で前記内部回路対応で設けられた第１の保護回路と、

前記複数の第１の保護回路全てに対して前記対電源とは独立した電源を供給する共通対電源端子と、

前記複数の内部回路にそれぞれ電源を供給する前記複数の対電源の第一電源端子に一方の電源端子を接続し、他方の電源端子を前記共通対電源端子の第二電源端子に接続するか、又は前記複数の対電源の第二電源端子に一方の電源端子を接続し、他方の電源端子を前記共通対電源端子の第一電源端子に接続して前記内部回路を静電電圧より保護する回路で前記複数の対電源対応で設けられた複数の第２の保護回路と、

を具備することを特徴とする静電破壊保護回路。

【請求項２】　前記全ての第１の保護回路に独立した別の対電源を供給する共通対電源端子を、前記複数の内部回路に電源を供給する複数の対電源端子のいずれかひとつの対電源端子と共用することを特徴とする請求項１に記載の静電破壊保護回路。

【請求項３】　前記複数の内部回路に電源を供給する複数の対電源端子の第一電源端子と第二電源端子間を接続して前記内部回路を静電電圧より保護する回路で前記複数の対電源対応で設けられた複数の第３の保護回路、及び前記全ての第１の保護回路に独立した別の対電源を供給する共通対電源端子の第一電源端子と第二電源端子間を接続して前記内部回路を静電電圧より保護する同第３の保護回路を設けたことを特徴とする請求項１又は２に記載の静電破壊保護回路。

【請求項４】　前記内部回路に電源を供給する対電源の数は３個以上とすることを特徴とする請求項１乃至３いずれかに記載の静電破壊保護回路。

【請求項５】　外部の信号入出力端子と、

対電源から電源を供給されて、前記信号入出力端子との間で信号の入出力を行う入出力回路と、

前記入出力回路と前記信号入出力端子との間に挿入されて前記信号入出力端子から侵入する静電電圧より前記入出力回路を保護する保護回路と、

前記対電源とは独立して前記保護回路に電源を供給する独立した別の対電源と、

を具備することを特徴とする静電破壊保護回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体集積回路に係り、特に入出力回路及び内部回路を外部からの静電電圧により破壊されないように保護する静電破壊保護回路に関する。

【０００２】

【従来の技術】近年、半導体装置は多ピン化／多電源化に伴い、チップ内部に図７に示すような第一回路群１０を複数取り込む構成となっている。この第一回路群１０は、外部の信号入出力端子（Ｉ／Ｏ　ＰＡＤ）と、信号を入出力する入出力回路１と、入出力回路１を外部からの静電破壊から保護する保護回路Ａから成り、その対電源（例えばＶＤＤ／ＧＮＤ）は入出力回路１も保護回路Ａも同一電源となっている回路である。

【０００３】図８は第二回路群を示した例である。第二回路群２０は、内部回路３に対して静電破壊保護の耐圧向上を目的に図７に示した第一回路群１０を具備し、その対電源ＶＤＤ用のパッド（ＰＡＤ）２１とＧＮＤ用のパッド（ＰＡＤ）２２間に保護回路Ｂを挿入している。

【０００４】図９は図８に示した第二回路群を用いて４対の異なる電源系（ＶＤＤ１／ＧＮＤ１～ＶＤＤ４／ＧＮＤ４）により動作する内部回路３－１～３－４を有する回路に静電破壊保護対策を施した回路を例示した図である。内部回路３－１～３－４の静電破壊保護対策として、第１回路群１０－１～１０－４を備えた第二回路群２０－１～２０－４が各対電源ＶＤＤ１／ＧＮＤ１～ＶＤＤ４／ＧＮＤ４に接続されている。更に、異なる電源系間の静電電圧から各内部回路３－１～３－４を保護するために、例えばＶＤＤ１は保護回路Ｃを介してＧＮＤ４に接続されるが如く、異なる電源系間を１２個の保護回路Ｃにより接続している。

【０００５】図１０は前記図９の回路例を半導体装置全体のレベルで表わした例である。この回路例から明らかな如く、自己電源系だけではなく、異種電源系間の静電破壊保護耐圧を向上させるため、各電源間全てに保護回路Ｃを挿入していることが分かる。これにより、保護回路Ｃの挿入領域は例えば内部回路３－２の領域に入り込んでおり、このため、内部回路３－２は凹多角形状となっている。しかし、このような従来の静電破壊保護回路の構成では以下のような問題が発生する。

【０００６】

【発明が解決しようとする課題】上記した複数の異なる電源系により動作する複数の内部回路を静電破壊から保護するための従来の静電破壊保護回路では図１０の（１）～（６）対応で、以下に述べるような問題があった。（１）異種電源系の全ての組み合わせで保護回路Ｃを入れなければ、静電破壊保護耐圧向上の効果は期待できないため、保護回路Ｃの数が独立電源系の数の増加に伴って急激に多くなってしまう。（２）保護回路Ｃの挿入領域は内部回路の領域に多いため、電源ラインの引き回しが複雑となる。（３）保護回路Ｃの挿入領域は内部回路の領域に多いため、内部回路が電源ノイズ等の影響

を受け易くなる。（４）保護回路Ｃの挿入領域は内部回路の領域に多いため、内部回路領域にデットスペースができやすい。（５）保護回路Ｃの挿入領域は内部回路の領域に多いため、内部回路領域が断片化（３－１Ａ，３－１Ｂ，３－１Ｃ）され集積度が低下する。（６）保護回路Ｃの挿入領域は内部回路の領域に多いため、内部回路領域が凹ラ角形状になり易く、集積度が低下する。

【０００７】本発明は、上述の如き従来の課題を解決するためになされたもので、その目的は、異種電源間の静電破壊保護用の保護回路の数を異種電源の数が増えても抑えることができ、それによって電源ラインの引き回しを簡素化し、内部回路がノイズの影響を受けないようにでき、且つ、デッドスペースを削減して集積度の低下を防止することができる静電破壊保護回路を提供することである。

【０００８】

【課題を解決するための手段】上記目的を達成するために、請求項１の発明の特徴は、対電源端子から電源が供給され、且つ外部の信号入出力端子に対し信号を入出力回路を介して入出力する内部回路を複数個有する回路にあって、前記入出力回路及び前記複数の内部回路を外部から侵入する静電電圧による破壊から保護する静電破壊保護回路において、前記入出力回路と前記信号入出力端子との間に挿入されて前記信号入出力端子から侵入する静電電圧より前記入出力回路を保護する回路で前記複数の内部回路対応で設けられた第１の保護回路と、前記複数の第１の保護回路全てに対して前記対電源とは独立した電源を供給する共通対電源端子と、前記複数の内部回路にそれぞれ電源を供給する前記複数の対電源の各第一電源端子に一方の電源端子を接続し、他方の電源端子を前記共通対電源端子の第二電源端子に接続するか、又は前記複数の対電源の各第二電源端子に一方の電源端子を接続し、他方の電源端子を前記共通対電源端子の第一電源端子に接続して前記内部回路を静電電圧より保護する回路で前記複数の対電源対応で設けられた複数の第２の保護回路とを具備することにある。

【０００９】請求項２の発明の特徴は、前記全ての第１の保護回路に独立した別の対電源を供給する共通対電源端子を、前記複数の内部回路に電源を供給する複数の対電源端子のいずれかひとつの対電源端子と共用することにある。

【００１０】請求項３の発明の特徴は、前記複数の内部回路に電源を供給する複数の対電源端子の各第一電源端子と各第二電源端子間を接続して前記内部回路を静電電圧より保護する回路で前記複数の対電源対応で設けられた複数の第３の保護回路、及び前記全ての第１の保護回路に独立した別の対電源を供給する共通対電源端子の第一電源端子と第二電源端子間を接続して前記内部回路を静電電圧より保護する同第３の保護回路を設けたことにある。

【００１１】請求項４の発明の特徴は、前記内部回路に電源を供給する対電源の数は３個以上とすることにある。

【００１２】請求項５の発明の特徴は、外部の信号入出力端子と、対電源から電源を供給されて、前記信号入出力端子との間で信号の入出力を行う入出力回路と、前記入出力回路と前記信号入出力端子との間に挿入されて前記信号入出力端子から侵入する静電電圧より前記入出力回路を保護する保護回路と、前記対電源とは独立して前記保護回路に電源を供給する独立した別の対電源とを具備することにある。

【００１３】本発明によれば、複数の独立した電源系を持つ半導体装置において、外部信号入出力端子と入出力回路との間に接続され、入出力回路を外部からの静電破壊電圧より保護するために設けられた第１の保護回路の対電源を共通の配線でバイアスすることにより、異種電源間に挿入する静電破壊保護用の第２の保護回路の数を削減する。これにより異種電源間に挿入する静電破壊保護用の保護回路間の電源配線を容易にでき、フロアプランの自由度を向上させることができる。

【００１４】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて説明する。図１は、本発明の静電破壊保護回路の第１の実施形態に係る構成を示した回路図である。但し、従来と同一構成要素には同一符号を付して説明する。対電源（ＶＤＤ１／ＧＮＤ１）～（ＶＤＤ４／ＧＮＤ４）から電源を供給されて動作する内部回路３－１～３－４の静電破壊保護として、第一回路群３０－１～３０－４を備えた第二回路群２０－１～２０－４が各対電源（ＶＤＤ１／ＧＮＤ１）～（ＶＤＤ４／ＧＮＤ４）対応で設けられ、且つ、異種電源間の静電電圧による入出力回路１－１～１－４及び内部回路３－１～３－４の破壊を防止するために、保護回路Ｃ（１）～保護回路Ｃ（８）が挿入されている。　ここで、上記した第一回路群３０の基本構成は図２を示した構成を有している。本例の第一回路群３０は、入出力回路１を保護する保護回路Ａが、内部回路３に電源を供給する対電源ＶＤＤとＧＮＤとは独立した別の対電源ＶＤＤとＧＮＤから電源を供給されるようになっており、その電源パッド（ＰＡＤ）８、９を備えている。但し、保護回路Ａは特許請求の範囲の第１の保護回路に相当し、保護回路Ｃは第２の保護回路に相当する。

【００１５】従って、上記した図１の回路では、第一回路群３０－１～３０－４の保護回路Ａに接続される対電源の端子が共通で、ＶＤＤ－ＥＳＤとＧＮＤ－ＥＳＤとなり、全ての保護回路ＡはＶＤＤ－ＥＳＤ用パッド（ＰＡＤ）４１とＧＮＤ－ＥＳＤ用パッド（ＰＡＤ）４２に接続されている。又、ＶＤＤ１用パッド（ＰＡＤ）１１、ＶＤＤ２用パッド（ＰＡＤ）１３、ＶＤＤ３用パッド（ＰＡＤ）１５、ＶＤＤ４用パッド（ＰＡＤ）１７に

一方の電源端子を接続された保護回路C（１），保護回路C（３），保護回路C（５），保護回路C（７）は、他方の電源端子をGND－ESDパッド（PAD）４２に接続されている。GND１用パッド（PAD）１２、GND２用パッド（PAD）１４、GND３用パッド（PAD）１６、GND４用パッド（PAD）１８に一方の電源端子を接続された保護回路C（２），保護回路C（４），保護回路C（６），保護回路C（８）は、他方の電源端子をVDD－ESD用パッド（PAD）４２に接続されている。

【００１６】次に本実施形態の動作について説明する。まず、保護回路A，B，Cはいずれも外部から侵入してきた静電電圧が入出力回路１－１～１－４や内部回路３－１～３－４に掛からないようにすることにより、これら回路を保護している。例えば、VDD－ESDを基準端子（静電電圧をチップ外に逃がす端子）として第二回路群２０－１に着目すると、対電源VDD１とGND１用のパッド１１、１２から侵入する静電電圧に対しては、保護回路C（１），（２）と第一回路群３０－１～３０－４の保護回路Aにより入出力回路１－１及び内部回路３－１が保護される。また、第一回路群３０－１のI／OPADよりの静電電圧に対しては、前記第一回路群３０－１の保護回路Aにより入出力回路１－１及び内部回路３－１が保護される。他の第二回路群２０－２～２０－４の対電源VDDとGND用のパッド１３～１５から侵入する静電電圧及び第二回路群２０－２～２０－４のI／OPADより侵入する静電電圧に対しても同様のことが言え、対応する保護回路Cと保護回路Aにより入出力回路１－２～１－４及び内部回路３－２～３－４が保護される。

【００１７】一方、共通対電源以外の電源PADが基準端子の場合に対しては、例えば電源VDD１が基準端子の場合、VDD２間には保護回路C（１）と保護回路C（３）の直列回路が挿入されていて、入出力回路及び内部回路を保護しており、他のケースも同様である。また、例えば電源VDD１とGND２間には保護回路C（１）と第一回路群３０－２の保護回路Aと保護回路C（４）の直列回路が挿入されて、入出力回路及び内部回路を保護しており、他のケースも同様である。

【００１８】本実施形態によれば、第一回路群３０の保護回路Aの基本構成を図２に示すように独立した別の対電源VDD／GNDに接続するようにし、図１の回路で、全ての第一回路群３０－１～３０－４の保護回路Aを共通の独立の対電源VDD－ESDとGND－ESD用のパッド４１、４２に接続する。また、保護回路（１）、（３）、（５）、（７）の一方の端子を内部回路３－１～３－４に電源を供給する対電源のVDD１、３、５、７に、他方の端子を共通対電源のGND－ESDに接続し、保護回路（２）、（４）、（６）、（８）の一方の端子を内部回路３－１～３－４に電源を供給する対電源のGND２、４、６、８に接続し、他方の端子を共通対電源のVDD－ESDに接続する構成により、異種電位電源の数が増えても保護回路Cの数を削減でき、しかも、少ない数の保護回路Cにより、全ての異種電位電源間から侵入する静電電圧に対して、内部回路３－１～３－４を保護することができる。

【００１９】又、全ての保護回路C（１）～（８）の他方の端子がVDD－ESDか、GND－ESD用のいずれかのパッド４１、４２に接続されるため、配線が簡素化され電源ラインの引き回しが短くなると共に、保護回路Aと入出力回路１に電源を供給する対電源を別にしたことと内部回路３－１～３－４の領域に保護回路Cを入り込ませないで済むようにしたため、内部回路３－１～３－４へのノイズの影響を無くすことができると共に、デッドスペースを削減して集積度の低下を防止することができる。

【００２０】図３は、本発明の静電破壊保護回路の第２の実施形態に係る構成を示した回路図である。本例の構成の保護回路Aの基本構成も図２に示したものと同一であり、全ての第一回路群３０の保護回路Aの独立対電源を共通にし、図１に示した第１の実施形態と同様の回路構成を有している。異なる点は、前記独立対電源を第１の実施形態のように別に設けず、VDD１とGND１と共用にしているところにある。このようにしても、入出力回路１－１～１－４及び内部回路３－１～３－４に対する静電破壊保護動作は全く第１の実施形態のそれと同様で、同様の効果があるが、前記独立対電源をVDD１及びGND１と共用にしているため、パッドの数を削減でき回路面積を縮小する上で多少とも有利である。

【００２１】図４は、本発明の静電破壊保護回路の第３の実施形態に係る構成を示した回路図である。本例の構成の保護回路Aの基本構成も図２に示したものと同一であり、全ての第一回路群３０の保護回路Aの独立対電源VDD－ESDとGND－ESDを共通にし、図１に示した第１の実施形態と同様の回路構成を有している。異なる点は、各内部回路３－１～３－４に電源を供給している各対電源VDD１／GND１～対電源VDD４／GND４間に保護回路B（請求の範囲の第３の保護回路に相当する）を挿入し、又、別の対電源VDD－ESD／GND－ESD間にも保護回路Bを接続することにより、上記第１、第２の実施形態に比較して静電破壊保護耐圧の向上を図ることができる。他の効果は第１の実施形態と同様である。

【００２２】図５は、図４に示した静電破壊保護回路の回路例を半導体装置全体のレベルで表わしたブロック図である。４個の対電源（VDD１／GND１）～（VDD４／GND４）に対して、８個の保護回路Cを有しているが、従来構成では４個の対電源に対して１２個の保護回路Cが必要であるため、明らかに保護回路Cの数を減らすことができる。これにより、保護回路Cの挿入領

域は内部回路３－１～３－４の外側となり、電源ラインの引き回しが簡素化され、内部回路領域にデットスペースがなく、内部回路領域が断片化されることもなく、また、内部回路領域が四角形状になっている。

【００２３】図６は対電源数の増加に対する電源間保護回路数の変化を本発明の構成と従来の構成で比較した特性図である。図から明らかなように対電源数が４個以上になると、本発明の効果が表れ、対電源数が多くなればなるほど、保護回路Ｃを削減する効果が著しくなることが分かる。

【００２４】尚、本発明は上記実施形態に限定されることなく、その要旨を逸脱しない範囲において、具体的な構成、機能、作用、効果において、他の種々の形態によっても実施することができる。

【００２５】

【発明の効果】以上詳細に説明したように、本発明の静電破壊保護回路によれば、入出力回路の対電源と保護回路Ａの対電源とを分離しているため、内部回路へのノイズ等の悪影響を抑えることができる。異種電源間に保護回路Ａ、Ｂ、Ｃを入れることにより電源間の寄生容量が増え、静電破壊保護耐圧を上げることができる。保護回路Ａに電源を供給する別の対電源を共有化することにより電源間の寄生容量が増えて静電破壊保護耐圧を上げることができる。保護回路Ａに使用している対電源を共有化するために異種電源の概念が消え、異種電源間に挿入する保護回路Ｃの数を削減でき、特に内部回路領域に入っていた保護回路Ｃを削減することにより、内部回路領域のフロアプランの自由度を上げることができ、更に、内部回路領域にデッドスペースを作らなくて済ますことができ、且つ半導体装置全体のサイズを小さくすることができる。

【図面の簡単な説明】

【図１】本発明の静電破壊保護回路の第１の実施形態に係る構成を示した回路図である。

【図２】図１に示した第一回路群の基本構成例を示した回路図である。

【図３】本発明の静電破壊保護回路の第２の実施形態に係る構成を示した回路図である。

【図４】本発明の静電破壊保護回路の第３の実施形態に係る構成を示した回路図である。

【図５】図４に示した静電破壊保護回路例を半導体装置全体のレベルで表わしたブロック図である。

【図６】対電源数の増加に対する電源間保護回路数の変化を本発明の構成と従来の構成で比較した特性図である。

【図７】従来の第一回路群の構成例を示した回路図である。

【図８】従来の第二回路群の構成例を示した回路図である。

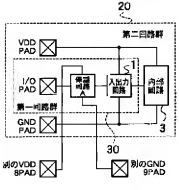
【図９】従来の静電破壊保護回路の構成例を示した回路図である。

【図１０】図９に示した静電破壊保護回路例を半導体装置全体のレベルで表わしたブロック図である。

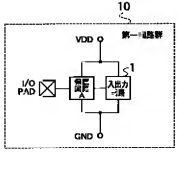
【符号の説明】

１－１～１－４　入出力回路
３－１～３－４　内部回路
１１　ＶＤＤ１用パッド（ＰＡＤ）
１２　ＧＮＤ１用パッド（ＰＡＤ）
１３　ＶＤＤ２用パッド（ＰＡＤ）
１４　ＧＮＤ２用パッド（ＰＡＤ）
１５　ＶＤＤ３用パッド（ＰＡＤ）
１６　ＧＮＤ３用パッド（ＰＡＤ）
１７　ＶＤＤ４用パッド（ＰＡＤ）
１８　ＧＮＤ４用パッド（ＰＡＤ）
２０、２０－１～２０－４　第二回路群
３０、３０－１～３０－４　第一回路群
４１　ＶＤＤ－ＥＳＤ用パッド（ＰＡＤ）
４２　ＧＮＤ－ＥＳＤ用パッド（ＰＡＤ）
Ａ、Ｂ、Ｃ　保護回路

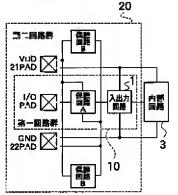
【図２】



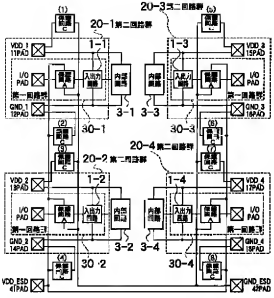
【図７】



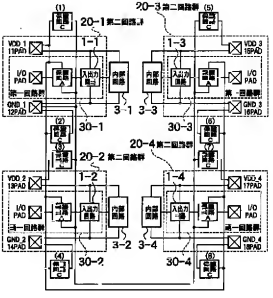
【図８】



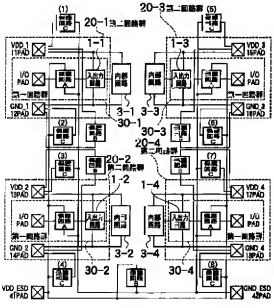
【図1】



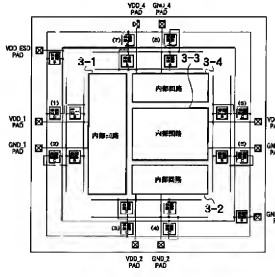
【図3】



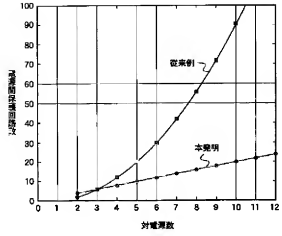
【図4】



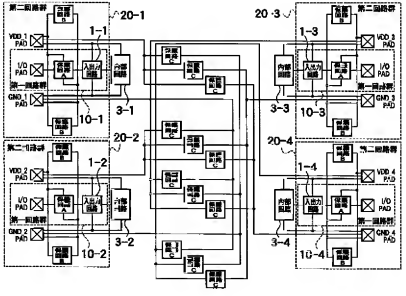
【図5】



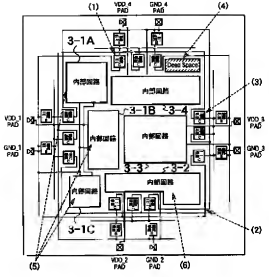
【図6】


100
90
80
70
60
50
40
30
20
10
0
0 1 2 3 4 5 6 7 8 9 10 11 12
対地雷数
従来例
本発明

【図9】


20-1
20-3
1-1
1-3
3-1
3-3
10-1
10-3
20-2
20-4
1-2
1-4
3-2
3-4
10-2
10-4

【図10】



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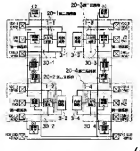
(54) ELECTROSTATIC BREAKDOWN PROTECTIVE CIRCUIT



(57)Abstract:

PROBLEM TO BE SOLVED: To suppress the number of protective circuits for protecting against an electrostatic breakdown between different types of power

supplies, even if the number of the different power supplies is increased.
SOLUTION: An electrostatic breakdown protective circuit comprises first protective circuits inserted between an input/output circuit and signal input/output terminal to protect the input/output circuits against an electrostatic voltage, coming from the signal input/output terminal to correspond to a plurality of internal circuits. Power is supplied from common paired power supply terminals independent of all the plurality of the first protective circuits. The one power supply terminal is connected to each VDD side terminal of the plurality of the paired power supplies for supplying the power to the plurality of the internal circuits. The other power supply terminal is connected to a GND side terminal of the common paired power terminal. Or one power supply terminal is connected to each GND side terminal of the plurality of the paired power supplies. The other power supply terminal is connected to the VDD side terminal of the common paired power supply terminal. Thus, a second protective circuit for protecting the internal circuit against the electrostatic voltage is provided, corresponding to the plurality of the paired power supplies. Thus, the number of the second protective circuits may not be increased even when the number of the different potential power supplies is increased.

LEGAL STATUS

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[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	

[Date of registration]

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[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]

[Claim 1] It is in the circuit which has two or more internal circuitries a power source is supplied from an opposite power supply terminal, and output and input a signal through an I/O circuit to an external signal input/output terminal. In the electrostatic-discharge protection network which protects said I/O circuit and said internal circuitry from destruction by the electrostatic electrical potential difference which invades from the outside The 1st protection network prepared by said internal-circuitry correspondence in the circuit which protects said I/O circuit from the electrostatic electrical potential difference which is inserted between said I/O circuits and said signal input/output terminals, and invades from said signal input/output terminal, The common opposite power supply terminal which supplies the power source which became independent of said opposite power source to said two or more 1st protection networks of all, One power

supply terminal is connected to the first power supply terminal of two or more of said opposite power sources which supply a power source to said two or more internal circuitries, respectively. [whether the power supply terminal of another side is connected to the second power supply terminal of said common opposite power supply terminal, and] Or two or more 2nd protection networks prepared by said two or more correspondences for a power source in the circuit which connects one power supply terminal to the second power supply terminal of two or more of said opposite power sources, connects the power supply terminal of another side to the first power supply terminal of said common opposite power supply terminal, and protects said internal circuitry from an electrostatic electrical potential difference, The electrostatic-discharge protection network characterized by providing.

[Claim 2] The electrostatic-discharge protection network according to claim 1 characterized by sharing the common opposite power supply terminal which supplies another opposite power source which became independent to said all 1st protection network with any one opposite power supply terminal of two or more opposite power supply terminals which supply a power source to said two or more internal circuitries.

[Claim 3] Two or more 3rd protection networks prepared by said two or more correspondences for a power source in the circuit which connects between the first power supply terminal of two or more opposite power supply terminals which supply a power source to said two or more internal circuitries, and the second power supply terminal, and protects said internal circuitry from an electrostatic electrical potential difference, And the electrostatic-discharge protection network according to claim 1 or 2 characterized by preparing this 3rd protection network which connects between the first power supply terminal of the common opposite power supply terminal which supplies another opposite power source which became independent to said all 1st protection network, and the second power supply terminal, and protects said internal circuitry from an electrostatic electrical potential difference.

[Claim 4] claim 1 characterized by making into three or more pieces the number of the opposite power sources which supply a power source to said internal circuitry thru/or 3 -- an electrostatic-discharge protection network given in either. [Claim 5] An external signal input/output terminal and the I/O circuit which a power source is supplied from an opposite power source, and output and input a signal between said signal input/output terminals, The protection network which protects said I/O circuit from the electrostatic electrical potential difference which is inserted between said I/O circuits and said signal input/output terminals, and invades from said signal input/output terminal, The electrostatic-discharge protection network characterized by providing another independent opposite power source which supplies a power source independently to said protection network with said opposite power source.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a semiconductor integrated circuit, especially relates to the electrostatic-discharge protection network which protects

an I/O circuit and an internal circuitry so that the electrostatic electrical potential difference from the outside may not break.

[0002]

[Description of the Prior Art] In recent years, the semiconductor device has composition which is crowded two or more picking in the first circuit group 10 as shown in the interior of a chip at drawing 7 with the formation of many pins / formation of many power sources. This first circuit group 10 consists of an external signal input/output terminal (I/O PAD), the I/O circuit 1 which output and input a signal, and the protection network A which protects the I/O circuit 1 from the electrostatic discharge from the outside, and that opposite power source (for example, VDD/GND) is a circuit where the I/O circuit 1 and the protection network A serve as the same power source.

[0003] Drawing 8 is the example which showed the second circuit group. The second circuit group 20 possesses the first circuit group 10 shown in drawing 7 to the internal circuitry 3 for the purpose of the improvement in a proof pressure of electrostatic-discharge protection, and is inserting the protection network B between the pad (PAD) 21 for the opposite power sources VDD, and the pad (PAD) 22 for GND.

[0004] Drawing 9 is drawing which illustrated the circuit which took the measures against electrostatic-discharge protection against the circuit which has the internal circuitry 3-1 to 3-4 which operates using the second circuit group shown in drawing 8 according to four pairs of different electrical power systems (VDD1/GND1-VDD4/GND4). As a cure against electrostatic-discharge protection of an internal circuitry 3-1 to 3-4, the second circuit group 20-1 to 20-4 equipped with the 1st circuit group 10-1 to 10-4 is connected to each set power-source VDD1/GND1-VDD4/GND4. Furthermore, in order to protect each internal circuitry 3-1 to 3-4 from the electrostatic electrical potential difference between different electrical power systems, VDD1 has connected between different electrical power systems by 12 protection networks C so that it may connect with GND4 through a protection network C.

[0005] Drawing 10 is the example which expressed the example of a circuit of said drawing 9 with the level of the whole semiconductor device. In order to raise the electrostatic-discharge protection pressure-proofing not only between a self-electrical power system but different-species electrical power systems so that clearly from this example of a circuit, it turns out that the protection network C is inserted in all between each power source. Thereby, the insertion field of a protection network C has entered the field of an internal circuitry 3-2, and, for this reason, the internal circuitry 3-2 has become reentering polygon-like. However, the following problems occur with the configuration of such a conventional electrostatic-discharge protection network.

[0006]

[Problem(s) to be Solved by the Invention] In the conventional electrostatic-discharge protection network for protecting two or more internal circuitries which operate according to the electrical power system from which the above-mentioned plurality differs from an electrostatic discharge, there was a problem which is described below by (1) - (6) correspondence of drawing 10 . (1) If a protection network C is not put in in all the combination of a different-species electrical power system, since the effectiveness of the improvement in an electrostatic-discharge protection proof pressure is not expectable, its number of protection networks C will increase rapidly with the increment in the number of independent source systems. (2) Since the field of an internal circuitry has many insertion fields of a protection network C, it becomes complicated taking about them power-source Rhine. (3) Since the field of an internal circuitry has many insertion fields of a protection network C, an internal circuitry becomes easy to be influenced of a power-source noise etc. (4) Since the field of an internal circuitry has many insertion fields of a protection network C, a DETTO tooth space tends to be made by them to an internal-circuitry field. (5) Since the field of an internal circuitry has many insertion fields of a protection network C, an internal-circuitry field is fragmented (3-1A, 3-1B, 3-1C), and a degree of integration falls. (6) Since the field of an internal circuitry has many insertion fields of a protection network C,

an internal-circuitry field tends to become reentering polygon-like, and a degree of integration falls.

[0007] It is what was made in order that this invention might solve the conventional technical problem like ****. The purpose The number of the protection networks for the electrostatic-discharge protection between different-species power sources can be stopped even if the number of different-species power sources increases. It is offering the electrostatic-discharge protection network which leading about of power-source Rhine is simplified by it, and an internal circuitry's can be prevented from being influenced of a noise, and can reduce dead space, and can prevent the fall of a degree of integration.

[0008]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the description of invention of claim 1 It is in the circuit which has two or more internal circuitries a power source is supplied from an opposite power supply terminal, and output and input a signal through an I/O circuit to an external signal input/output terminal. In the electrostatic-discharge protection network which protects said I/O circuit and said two or more internal circuitries from destruction by the electrostatic electrical potential difference which invades from the outside The 1st protection network prepared by said two or more internal-circuitry correspondences in the circuit which protects said I/O circuit from the electrostatic electrical potential difference which is inserted between said I/O circuits and said signal input/output terminals, and invades from said signal input/output terminal, The common opposite power supply terminal which supplies the power source which became independent of said opposite power source to said two or more 1st protection networks of all, One power supply terminal is connected to each first power supply terminal of two or more of said opposite power sources which supply a power source to said two or more internal circuitries, respectively. [whether the power supply terminal of another side is connected to the second power supply terminal of said common opposite power supply terminal, and] Or it is in providing two or more 2nd protection

networks prepared by said two or more correspondences for a power source in the circuit which connects one power supply terminal to each second power supply terminal of two or more of said opposite power sources, connects the power supply terminal of another side to the first power supply terminal of said common opposite power supply terminal, and protects said internal circuitry from an electrostatic electrical potential difference.

[0009] The description of invention of claim 2 is to share the common opposite power supply terminal which supplies another opposite power source which became independent to said all 1st protection network with any one opposite power supply terminal of two or more opposite power supply terminals which supply a power source to said two or more internal circuitries.

[0010] every of two or more opposite power supply terminals with which the description of invention of claim 3 supplies a power source to said two or more internal circuitries -- the first power supply terminal and every -- two or more 3rd protection networks prepared by said two or more correspondences for a power source in the circuit which connects between the second power supply terminal and protects said internal circuitry from an electrostatic electrical potential difference -- And it is in having prepared this 3rd protection network which connects between the first power supply terminal of the common opposite power supply terminal which supplies another opposite power source which became independent to said all 1st protection network, and the second power supply terminal, and protects said internal circuitry from an electrostatic electrical potential difference.

[0011] The number of opposite power sources with which the description of invention of claim 4 supplies a power source to said internal circuitry is to consider as three or more pieces.

[0012] The I/O circuit which a power source is supplied to the description of invention of claim 5 from an external signal input/output terminal and an external opposite power source, and outputs and inputs a signal between said signal input/output terminals, The protection network which protects said I/O circuit from

the electrostatic electrical potential difference which is inserted between said I/O circuits and said signal input/output terminals, and invades from said signal input/output terminal, and said opposite power source are to provide another independent opposite power source which supplies a power source independently to said protection network.

[0013] According to this invention, in a semiconductor device with the electrical power system which plurality became independent of, it connects between an external signal input/output terminal and an I/O circuit, and the number of the 2nd protection networks for electrostatic-discharge protection inserted between different-species power sources is reduced by carrying out bias of the opposite power source of the 1st protection network prepared in order to protect an I/O circuit from the electrostatic-discharge electrical potential difference from the outside with common wiring. Power-source wiring between the protection networks for the electrostatic-discharge protection which this inserts between different-species power sources can be made easy, and the degree of freedom of a floor plan can be raised.

[0014]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing. Drawing 1 is the circuit diagram having shown the configuration concerning the 1st operation gestalt of the electrostatic-discharge protection network of this invention. However, the same sign is attached and explained to the same component as the former. As electrostatic-discharge protection of the internal circuitry 3-1 to 3-4 which a power source is supplied and operates from - for a power source (VDD1/GND1) (VDD4/GND4) The second circuit group 20-1 to 20-4 equipped with the first circuit group 30-1 to 30-4 is formed by each set power source (VDD1/GND1) - (VDD4/GND4) correspondence. And in order to prevent destruction of the I/O circuit 1-1 to 1-4 by the electrostatic electrical potential difference between different-species power sources, and an internal circuitry 3-1 to 3-4, the protection network C (1) - the protection network C (8) are inserted. Here, the above-mentioned basic

configuration of the first circuit group 30 has the configuration which showed drawing 2 . The power source was supplied to the first circuit group 30 of this example from another independent opposite power sources VDD and GND, and, as for the opposite power sources VDD and GND with which the protection network A which protects the I/O circuit 1 supplies a power source to an internal circuitry 3, it is equipped with the power-source pads (PAD) 8 and 9. However, a protection network A is equivalent to the 1st protection network of a claim, and a protection network C is equivalent to the 2nd protection network.

[0015] Therefore, in the above-mentioned circuit of drawing 1 , the terminal of an opposite power source connected to the protection network A of the first circuit group 30-1 to 30-4 is common, and serves as VDD-ESD and GND-ESD, and all the protection networks A are connected to the pad (PAD) 41 for VDD-ESD, and the pad (PAD) 42 for GND-ESD. Moreover, as for the protection network C (1) where one power supply terminal was connected to the pad (PAD) 11 for VDD1, the pad (PAD) 13 for VDD2, the pad (PAD) 15 for VDD3, and the pad (PAD) 17 for VDD4, the protection network C (3), the protection network C (5), and the protection network C (7), the power supply terminal of another side is connected to the GND-ESD pad (PAD) 42. As for the protection network C (2) where one power supply terminal was connected to the pad (PAD) 12 for GND1, the pad (PAD) 14 for GND2, the pad (PAD) 16 for GND3, and the pad (PAD) 18 for GND4, the protection network C (4), the protection network C (6), and the protection network C (8), the power supply terminal of another side is connected to the pad (PAD) 42 for VDD-ESD.

[0016] Next, actuation of this operation gestalt is explained. First, protection networks A, B, and C have protected these circuits, when making it the electrostatic electrical potential difference which has all invaded from the outside built neither over the I/O circuit 1-1 to 1-4, nor an internal circuitry 3-1 to 3-4. For example, if its attention is paid to VDD-ESD at the second circuit group 20-1 as a reference terminal (terminal which misses an electrostatic electrical potential difference out of a chip), to the electrostatic electrical potential difference which

invades from the pads 11 and 12 the opposite power source VDD1 and for GND1, the I/O circuit 1-1 and an internal circuitry 3-1 will be protected by the protection network A of a protection network C (1), (2), and the first circuit group 30-1 to 30-4. Moreover, to the electrostatic electrical potential difference from I/OPAD of the first circuit group 30-1, the I/O circuit 1-1 and an internal circuitry 3-1 are protected by the protection network A of said first circuit group 30-1. The same thing can be said also to the electrostatic electrical potential difference which invades from I/OPAD of the electrostatic electrical potential difference which invades from the opposite power source VDD of other second circuit groups 20-2 to 20-4, and the pads 13-15 for GND, and the second circuit group 20-2 to 20-4, and the I/O circuit 1-2 to 1-4 and an internal circuitry 3-2 to 3-4 are protected by a corresponding protection network C and a corresponding protection network A.

[0017] On the other hand, to the case where power sources PAD other than a common opposite power source are reference terminals, when a power source VDD1 is a reference terminal, for example, among VDD2, the series circuit of a protection network C (1) and a protection network C (3) is inserted, the I/O circuit and the internal circuitry are protected, and other cases are the same. Moreover, for example among power sources GND [VDD1 and] 2, the protection network C (1), the protection network A of the first circuit group 30-2, and the series circuit of a protection network C (4) were inserted, the I/O circuit and the internal circuitry are protected, and other cases are the same.

[0018] According to this operation gestalt, the basic configuration of the protection network A of the first circuit group 30 is connected to another VDD/GND for a power source which became independent as shown in drawing 2 , and the protection network A of all the first circuit groups 30-1 to 30-4 is connected to the pads 41 and 42 common independent VDD-ESD for a power source, and for GND-ESD in the circuit of drawing 1 . One terminal of a protection network (1), (3), (5), and (7) to moreover, VDD 1, 3, 5, and 7 of the opposite power source which supplies a power source to an internal circuitry 3-1 to 3-4 An other-end child is connected to GND-ESD of a common opposite power

source. A protection network (2), By the configuration which connects one terminal of (4), (6), and (8) to GND 2, 4, 6, and 8 of the opposite power source which supplies a power source to an internal circuitry 3-1 to 3-4, and connects an other-end child to VDD-ESD of a common opposite power source Even if the number of different-species potential power sources increases, the number of protection networks C can be reduced, and an internal circuitry 3-1 to 3-4 can be protected to the electrostatic electrical potential difference which moreover invades from between all different-species potential power sources by a small number of protection networks C.

[0019] Moreover, since the other-end child of all protection network C (1) - (8) is connected to one for VDD-ESD and GND-ESD of the pads 41 and 42, while wiring is simplified and leading about of power-source Rhine becomes short Since it was made not to make a protection network C enter the field of having set aside the opposite power source which supplies a power source to a protection network A and the I/O circuit 1, and an internal circuitry 3-1 to 3-4, While being able to lose the effect of the noise to an internal circuitry 3-1 to 3-4, dead space can be reduced and the fall of a degree of integration can be prevented.

[0020] Drawing 3 is the circuit diagram having shown the configuration concerning the 2nd operation gestalt of the electrostatic-discharge protection network of this invention. The basic configuration of the protection network A of the configuration of this example is also the same as that of what was shown in drawing 2 , the independent opposite power source of the protection network A of all the first circuit groups 30 is carried out in common, and it has the same circuitry as the 1st operation gestalt shown in drawing 1 . A different point does not independently establish said independent opposite power source like the 1st operation gestalt, but is in the place set to VDD1 and GND1 at common use. Although there is same effectiveness, since said independent opposite power source is set to VDD1 and GND1 at common use, when the number of pads can be reduced and circuit area is reduced, some are advantageous [the

electrostatic-discharge protected operation to the I/O circuit 1-1 to 1-4 and an internal circuitry 3-1 to 3-4 is completely the same as that of it of the 1st operation gestalt, and], even if such.

[0021] Drawing 4 is the circuit diagram having shown the configuration concerning the 3rd operation gestalt of the electrostatic-discharge protection network of this invention. The basic configuration of the protection network A of the configuration of this example is also the same as that of what was shown in drawing 2 , independent opposite power-source VDD-ESD and GND-ESD of a protection network A of all the first circuit groups 30 are carried out in common, and it has the same circuitry as the 1st operation gestalt shown in drawing 1 . A different point inserts a protection network B (it is equivalent to the 3rd protection network of a claim) among each internal-circuitry 3-1 - 3 each set power sources VDD1/GND1 which supply the power source to -4 - the pair power sources VDD4/GND 4. Moreover, as compared with the above 1st and the 2nd operation gestalt, improvement in electrostatic-discharge protection pressure-proofing can be aimed at by connecting a protection network B also between another VDD-ESD/GND-ESD for a power source. Other effectiveness is the same as the 1st operation gestalt.

[0022] Drawing 5 is the block diagram which expressed with the level of the whole semiconductor device the example of a circuit of the electrostatic-discharge protection network shown in drawing 4 . Although it has eight protection networks C to - for four power sources (VDD1/GND1) (VDD4/GND4), since 12 protection networks C are required, with a configuration, the number of protection networks C can be conventionally reduced clearly to four opposite power sources. Thereby, the internal-circuitry field has become square-like, without the insertion field of a protection network C serving as an outside of an internal circuitry 3-1 to 3-4, and simplifying leading about of power-source Rhine, and there being no DETTO tooth space in an internal-circuitry field, and fragmenting an internal-circuitry field.

[0023] Drawing 6 is the property Fig. which compared change of the number of

the protection networks between power sources to the increment in the number of opposite power sources with the configuration of this invention, and the conventional configuration. When the number of opposite power sources becomes four or more pieces so that clearly from drawing, if the effectiveness of this invention appears and the number of opposite power sources increases, it turns out that the effectiveness which reduces protection networks C becomes remarkable indeed.

[0024] In addition, this invention can be carried out according to other various gestalten in a concrete configuration, a function, an operation, and effectiveness in the range which does not deviate from the summary, without being limited to the above-mentioned operation gestalt.

[0025]

[Effect of the Invention] Since the opposite power source of an I/O circuit and the opposite power source of a protection network A are separated according to the electrostatic-discharge protection network of this invention as explained to the detail above, bad influences, such as a noise to an internal circuitry, can be stopped. By putting in protection networks A, B, and C between different-species power sources, the parasitic capacitance between power sources can increase and electrostatic-discharge protection pressure-proofing can be raised. By share-izing another opposite power source which supplies a power source to a protection network A, the parasitic capacitance between power sources can increase and electrostatic-discharge protection pressure-proofing can be raised. By the idea of a different-species power source disappearing, in order to share-ize the opposite power source currently used for a protection network A, and being able to reduce the number of the protection networks C inserted between different-species power sources, and reducing the protection networks C included in especially an internal-circuitry field, further, the degree of freedom of the floor plan of an internal-circuitry field can be raised, and it can be finished [cannot make dead space, and] to an internal-circuitry field, and size of the whole semiconductor device can be made small.

[Translation done.]

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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram having shown the configuration concerning the 1st operation gestalt of the electrostatic-discharge protection network of this invention.
[Drawing 2] It is the circuit diagram having shown the example of a basic configuration of the first circuit group shown in drawing 1 .
[Drawing 3] It is the circuit diagram having shown the configuration concerning the 2nd operation gestalt of the electrostatic-discharge protection network of this invention.
[Drawing 4] It is the circuit diagram having shown the configuration concerning the 3rd operation gestalt of the electrostatic-discharge protection network of this invention.
[Drawing 5] It is the block diagram which expressed with the level of the whole semiconductor device the example of an electrostatic-discharge protection network shown in drawing 4 .
[Drawing 6] It is the property Fig. which compared change of the number of the protection networks between power sources to the increment in the number of

opposite power sources with the configuration of this invention, and the conventional configuration.

[Drawing 7] It is the circuit diagram having shown the example of a configuration of the conventional first circuit group.

[Drawing 8] It is the circuit diagram having shown the example of a configuration of the conventional second circuit group.

[Drawing 9] It is the circuit diagram having shown the example of a configuration of the conventional electrostatic-discharge protection network.

[Drawing 10] It is the block diagram which expressed with the level of the whole semiconductor device the example of an electrostatic-discharge protection network shown in drawing 9 .

[Description of Notations]

1-1 to 1-4 I/O circuit

3-1 to 3-4 Internal circuitry

11 Pad for VDD1 (PAD)

12 Pad for GND1 (PAD)

13 Pad for VDD2 (PAD)

14 Pad for GND2 (PAD)

15 Pad for VDD3 (PAD)

16 Pad for GND3 (PAD)

17 Pad for VDD4 (PAD)

18 Pad for GND4 (PAD)

20 20-1 to 20-4 The second circuit group

30 30-1 to 30-4 The first circuit group

41 Pad for VDD-ESD (PAD)

42 Pad for GND-ESD (PAD)

A, B, C Protection network

[Translation done.]

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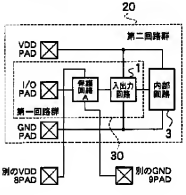
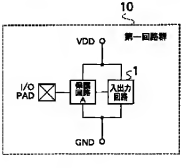
3.In the drawings, any words are not translated.

DRAWINGS

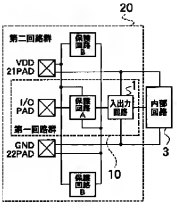
[Drawing 2]



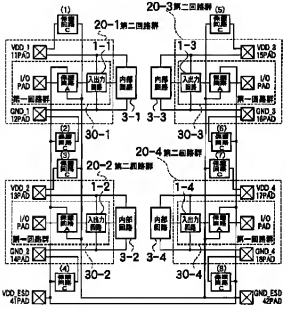
[Drawing 7]



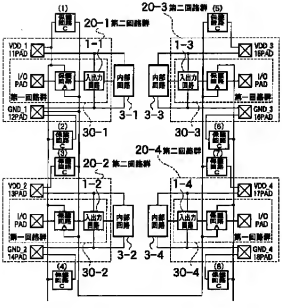
[Drawing 8]



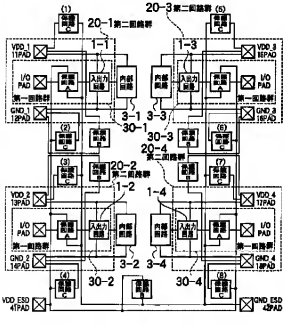
[Drawing 1]



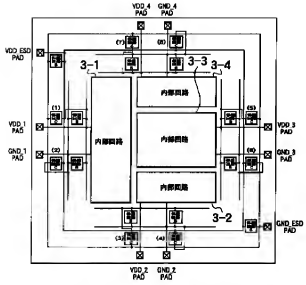
[Drawing 3]



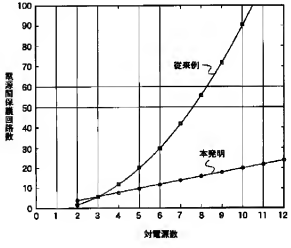
[Drawing 4]



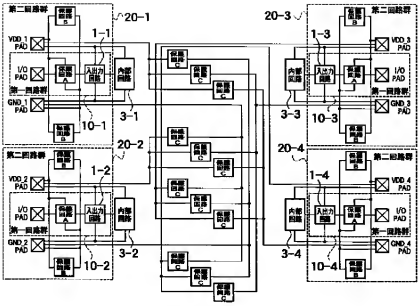
[Drawing 5]



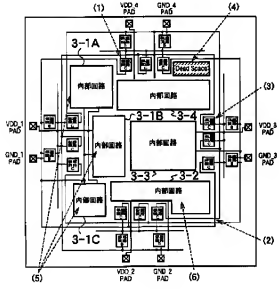
[Drawing 6]



[Drawing 9]



[Drawing 10]



[Translation done.]